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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/604,255

07/07/2003

Michael P. Belyansky

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INTERNATIONAL BUSINESS MACHINES CORPORATION

DEPT. 18G

BLDG. 300-482

2070 ROUTE 52

HOPEWELL JUNCTION, NY 12533

EXAMINER

SMOOT, STEPHEN W

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/604,255

Applicant(s)

BELYANSKY ET AL.

Examiner

Stephen W. Smoot

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 07 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-6,11-15,17,19 and 20 is/are rejected.
- 7) ☒ Claim(s) 3, 7-10, 16, 18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 July 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)                | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>7-7-03</u> .  | 6) <input type="checkbox"/> Other: _____                                    |

### **DETAILED ACTION**

This Office action is in response to application papers filed on 07 July 2003.

#### ***Drawings***

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

10 in Figs. 1-5;

110 in Figs. 1-2; and

155 in Fig. 3.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified

and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because in Fig. 6B, reference character "130" has been used to designate both a dotted oval and a vertical transistor and reference character "132" has been used to designate both a lower electrode and a buried strap (see paragraph [0045]).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Specification***

3. The disclosure is objected to because of the following informalities:

Fig. 4 is not described in the "Detailed Description" section.

Appropriate correction is required.

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification needs to be amended to provide antecedence for "a step of performing a bottle etch precedes the step of depositing a thermally stable filling material" as claimed in original claims 11, 13.

#### ***Claim Objections***

5. Claims 4, 12 are objected to because of the following informality:

In claim 4, line 2, change "heating" to --annealing-- for proper antecedence to claim 3; and

In claim 12, line 2, change "heating" to --annealing-- for proper antecedence to claim 1.

Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 4, 17, 19-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4, line 3, the term "the step of trench filling" does not particularly point out if this is with reference to the "depositing a thermally stable filler material" step of claim 1, line 4 or the "depositing a conductive electrode" step of claim 1, line 11.

In claim 17, line 3, the term "the step of trench filling" does not particularly point out if this is with reference to the "depositing a thermally stable filler material" step of claim 14, lines 5-6 or the "depositing a conductive electrode" step of claim 14, line 12.

Claims 19-20 are rejected under 35 U.S.C. 112, second paragraph, because they depend on claim 17.

### ***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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9. Claims 1-2, 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Shrems (US 6,008,104).

Referring to Figs. 4A-4H and column 7, line 21 to column 11, line 67, Shrems discloses a method for forming a DRAM cell that includes a deep trench capacitor. The deep trench (408) is formed in a substrate (401) by RIE and is partially filled with a sacrificial poly layer (452) that is recessed for defining the bottom of a collar (468). The collar (468) is formed by depositing an oxide layer (467) (e.g. LPCVD using TEOS), densifying the oxide layer (467) by annealing in an ambient that may include oxygen, and opening the collar (468) by RIE. The sacrificial poly layer (452) is then removed and the exposed substrate (401) is then doped to form a buried plate (465). The trench (408) is then lined with a dielectric layer (464) and filled with doped polysilicon (461) to form the upper electrode of the capacitor. A transistor (410) with bitline (485) is subsequently formed over the trench capacitor.

These are all of the limitations set forth in claims 1-2, 14-15 of the applicant's invention.

10. Claims 1-2, 11, 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Lutzen (US 2002/0036310 A1).

Referring to Figs. 3A-3I and paragraphs [0063] to [0070], Lutzen discloses a method for forming a DRAM cell that includes a trench capacitor. The trench is formed in a substrate (S1) by anisotropic etching followed by a second etching operation to widen the lower trench region as shown in Fig. 3C. The trench is then filled with

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polysilicon (S6), which is recessed by an etching back step for defining the bottom of a collar (S7). The collar (S7) is formed by depositing a conformal oxide layer (S7), which implies annealing in an oxygen ambient, followed by an anisotropic etching step. The polysilicon layer (S6) is then removed and the exposed substrate (S1) is then doped to form a buried plate (S8). The trench is then lined with a dielectric layer (S9) and filled with doped polysilicon (S10) to form the upper electrode of the capacitor. A transistor (2) with bitline (6) is subsequently formed over the trench capacitor as shown in Fig. 2.

These are all of the limitations set forth in claims 1-2, 11, 14-15 of the applicant's invention.

11. Claims 1, 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Tews et al. (US 6,670,235 B1).

Referring to Figs. 2-5 and column 3, line 57 to column 5, line 55, Tews et al. discloses a method for forming a trench capacitor for DRAMs. The trench is formed in a substrate by RIE and then filled with a poly fill (21), which is subsequently recessed for defining the bottom of a collar (23). The collar (23) is a nitride (i.e. a high k material) that is formed by a process that includes oxidizing exposed portions of a nitride layer (20) while the poly fill (21) is present. The poly fill layer (21) is then stripped and the exposed substrate is then doped to form a buried plate (11). The trench is then lined with a dielectric layer (14) and filled with doped trench poly fill (24) to form the upper electrode of the capacitor.

These are all of the limitations set forth in claims 1, 5 of the applicant's invention.



***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lutzen (US 2002/0036310 A1) as applied to claim 2 above, and further in view of Tews et al. (US 6,670,235 B1).

As shown above, Lutzen anticipates claim 2 of the applicant's invention. However, Lutzen lacks the further limitation to claim 2 set forth in claim 6 of the applicant's invention, which is to deposit high k spacers. Tews et al. teach a trench capacitor with a collar that includes nitride layers (see column 5, lines 26-37).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Lutzen and Tews et al. in order to use a collar that includes nitride as taught by Tews et al. Tews et al. recognize that a high k collar has the advantage of suppressing vertical parasitic capacitance effects (see column 5, lines 6-18).

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14. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lutzen (US 2002/0036310 A1) as applied to claims 1, 11 above, and further in view of Koscielniak et al. (US 6,329,698 B1).

As shown above, Lutzen anticipates claims 1, 11 of the applicant's invention. However, Lutzen lacks the further limitation to claim 1 set forth in claim 12 of the applicant's invention, which is to form their conformal collar oxide layer by using a low pressure deposition at a temperature below 800 degrees C. Claim 13, which depends on claim 12, has the same limitation as claim 11. Koscielniak et al. teach the formation of a conformal silicon dioxide spacer by LPCVD at a temperature ranging from 300 to 500 degrees C (see column 8, lines 4-25).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Lutzen and Koscielniak et al. in order to form the conformal collar oxide layer using LPCVD as taught by Koscielniak et al. Koscielniak et al. show that LPCVD is one known way to conformally deposit silicon dioxide (see column 8, lines 4-25).

***Allowable Subject Matter***

15. Claims 3, 7-10, 16, 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. The following is a statement of reasons for the indication of allowable subject matter:

- Claims 3, 7, 16, 18 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of forming a trench capacitor that includes the step of forming insulating spacers on the trench sidewalls above a capacitor top level by atomic layer deposition at a temperature of less than 500 degrees C, combined with the step of annealing sacrificial filler material in an oxidizing ambient; and
- Claims 8-10 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of forming a trench capacitor that includes the step of forming insulating spacers on the trench sidewalls above a capacitor top level, combined with the step of annealing sacrificial filler material in an oxidizing ambient, wherein the spacers are formed by depositing a material selected from the group comprising aluminum oxide, hafnium oxide, zirconium oxide, lanthanum oxide, and their silicates.

### ***Conclusion***

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wei and Wei et al. teach methods for forming trench capacitors.

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Seidl et al. and Gutsche et al. teach methods for forming trench capacitors that utilize high k dielectrics.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

*Stephen W. Smoot*  
Patent Examiner  
Art Unit 2813